IN THE CLAIMS

Please cancel Claims 1-66 (Cancelled).

67. (Currently amended) A semiconductor device comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer;

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline semiconductor substrate;~~

~~an oxide layer formed overlying the substrate;~~

~~a monocrystalline compound semiconductor layer formed overlying the oxide layer;~~ and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer,

wherein the tunnel diode comprises an intraband tunnel diode,

wherein the tunnel diode comprises a quantum well layer sandwiched between first and second tunnel barrier layers and the first and second tunnel barrier layers are sandwiched between an injection layer and a collection layer,

wherein the quantum well layer comprises GaAs and the first and second tunnel barrier layers comprise a material selected from AlGaAs and AlAs

said device further comprising a monocrystalline buffer layer interposed between the oxide layer and the monocrystalline compound semiconductor layer, and

wherein the oxide layer comprises an alkali earth metal titanate and the buffer layer comprises a material selected from the group consisting of GaAs and AlGaAs.

68. (Previously presented) The semiconductor device of claim 67 wherein the quantum well layer and the first and second tunnel barrier layers are not intentionally doped.

69. (Previously presented) The semiconductor device of claim 67 wherein the injection layer and the collection layer each comprise GaAs.

70. (Previously presented) The semiconductor device of claim 69 wherein the injection layer and the collection layer are each impurity doped.

71. (Previously presented) The semiconductor device of claim 70 further comprising first and second contact layers contacting the injection layer and the collection layer, respectively, the first and second contact layers comprising monocrystalline GaAs more heavily impurity doped than the injection layer and the collection layer.

72. (Previously presented) The semiconductor device of claim 67 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

73. (Currently amended) A semiconductor device comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer;

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline semiconductor substrate;~~

~~an oxide layer formed overlying the substrate;~~

~~a monocrystalline compound semiconductor layer formed overlying the oxide layer;~~

and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer,

wherein the tunnel diode comprises an intraband tunnel diode,

wherein the tunnel diode comprises a quantum well layer sandwiched between first and second tunnel barrier layers and the first and second tunnel barrier layers are sandwiched between an injection layer and a collection layer,

wherein the quantum well layer comprises GaAs and the first and second tunnel barrier layers comprise a material selected from AlGaAs and AlAs, and

wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

74. (Previously presented) The semiconductor device of claim 73 wherein the substrate comprises silicon.

75. (Previously presented) The semiconductor device of claim 74 further comprising a digital circuit formed at least partially within the substrate and coupled to the tunnel diode.

76. (Previously presented) The semiconductor device of claim 67 wherein the quantum well layer comprises InGaAs and the first and second tunnel barrier layers comprise AlAs.

77. (Previously presented) The semiconductor device of claim 76 wherein the injection layer and the collection layer each comprise InGaAs.

78. (Previously presented) The semiconductor device of claim 77 further comprising first and second contact layers contacting the injection layer and the collection layer, respectively, the first and second contact layers comprising heavily impurity doped monocrystalline InGaAs.

79. (Previously presented) The semiconductor device of claim 77 further comprising a monocrystalline buffer layer between the oxide layer and the monocrystalline compound semiconductor layer.

80. (Previously presented) The semiconductor device of claim 79 wherein the buffer layer comprises a material selected from the group consisting of InP and InAlAs.

81. (Currently amended) A semiconductor device comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer;

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline semiconductor substrate;~~

~~an oxide layer formed overlying the substrate;~~

~~a monocrystalline compound semiconductor layer formed overlying the oxide layer;~~

and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer,

wherein the tunnel diode comprises an intraband tunnel diode,

wherein the tunnel diode comprises a quantum well layer sandwiched between first and second tunnel barrier layers and the first and second tunnel barrier layers are sandwiched between an injection layer and a collection layer,

wherein the quantum well layer comprises InGaAs and the first and second tunnel barrier layers comprise AlAs,

wherein the injection layer and the collection layer each comprise InGaAs,

said device further comprising a monocrystalline buffer layer between the oxide layer and the monocrystalline compound semiconductor layer,

wherein the buffer layer comprises a material selected from the group consisting of InP and InAlAs, and

wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal zirconates and alkali earth metal hafnates.

82. (Previously presented) The semiconductor device of claim 67 wherein the oxide layer comprises an amorphous oxide layer.

83. (Previously presented) The semiconductor device of claim 82 wherein the oxide layer comprises an amorphous oxide formed epitaxially as a monocrystalline oxide layer and subsequently heat treated to convert the monocrystalline oxide to an amorphous oxide.

84. (Previously presented) The semiconductor device of claim 73 wherein the oxide layer comprises an amorphous oxide layer.

85. (Previously presented) The semiconductor device of claim 84 wherein the oxide layer comprises an amorphous oxide formed epitaxially as a monocrystalline oxide layer and subsequently heat treated to convert the monocrystalline oxide to an amorphous oxide.

86. (Cancelled)

87. (Cancelled)

88. (Currently amended) A semiconductor device comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer;

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline semiconductor substrate;~~

~~an oxide layer formed overlying the substrate;~~

~~a monocrystalline compound semiconductor layer formed overlying the oxide layer;~~

and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer,

wherein the tunnel diode comprises an interband tunnel diode,

wherein the tunnel diode comprises first and second quantum well layers spaced apart by a barrier layer and the first and second quantum well layers are sandwiched between first and second carrier supply layers,

wherein the quantum well layers comprise InGaAs and the barrier layer comprises InAlAs,

wherein the first carrier supply layers comprise a layer of n-doped InGaAs and a layer of n-doped InAlAs with the layer of n-doped InAlAs in contact with the first quantum well layer and the second carrier supply layers comprise a layer of p-doped InGaAs and a layer of p-doped InAlAs with the layer of p-doped InAlAs in contact with the second quantum well layer,

said device further comprising a buffer layer comprising a material selected from the group consisting of InP and InAlAs interposed between the oxide layer and the monocrystalline compound semiconductor layer.

89. (Previously presented) The semiconductor device of claim 88 wherein the quantum well layers and the barrier layer are not intentionally doped.

90. (Previously presented) The semiconductor device of claim 88 wherein the oxide layer comprises an oxide selected from the group consisting of alkali earth metal zirconates and alkali earth metal hafnates.

91. (Previously presented) The semiconductor device of claim 88 wherein the quantum well layers comprise InGaAs and the barrier layer comprises GaAs.

92. (Previously presented) The semiconductor device of claim 88 wherein the first carrier supply layer comprises n-doped GaAs and the second carrier supply layer comprises p-doped GaAs.

93. (Currently Amended) A semiconductor device comprising:

a) a monocrystalline Group IV substrate:

b) a layer of amorphous oxide of Group IV in contact with said substrate;

c) a monocrystalline metal oxide and/or metal nitride layer overlying the amorphous layer;

d) a metal or metal oxide capping layer in contact with said monocrystalline metal oxide and/or metal nitride layer;

e) a compound semiconductor template layer in contact with said capping layer;

f) a monocrystalline compound semiconductor layer in contact with said template layer

~~a monocrystalline semiconductor substrate;~~

~~an oxide layer formed overlying the substrate;~~

~~a monocrystalline compound semiconductor layer formed overlying the oxide layer;~~

and

a tunnel diode formed at least partially in the monocrystalline compound semiconductor layer,

wherein the tunnel diode comprises an interband tunnel diode,

wherein the tunnel diode comprises first and second quantum well layers spaced apart by a barrier layer and the first and second quantum well layers are sandwiched between first and second carrier supply layers,

wherein the quantum well layers comprise InGaAs and the barrier layer comprises InAlAs,

wherein the first carrier supply layer comprises n-doped GaAs and the second carrier supply layer comprises p-doped GaAs,

said device further comprising a buffer layer comprising GaAs interposed between the oxide layer and the monocrystalline compound semiconductor layer.

94. (Previously presented) The semiconductor device of claim 93 wherein the oxide layer comprises an alkali earth metal titanate.

95. (Previously presented) The semiconductor device of claim 94 wherein the oxide layer comprises $Ba_xSr_{1-x}TiO_3$ where x ranges from 0 to 1.

96. (Previously presented) The semiconductor device of claim 67 wherein the substrate comprises silicon.

97. (Previously presented) The semiconductor device of claim 96 further comprising an amorphous silicon oxide formed underlying the oxide layer.

98. (Previously presented) The semiconductor device of claim 67 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.

99. (Previously presented) The semiconductor device of claim 83 wherein the substrate comprises silicon.

100. (Previously presented) The semiconductor device of claim 99 further comprising an amorphous silicon oxide formed underlying the oxide layer.

101. (Cancelled)

102. (Previously presented) The semiconductor device of claim 88 wherein the substrate comprises silicon.

103. (Previously presented) The semiconductor device of claim 102 further comprising an amorphous silicon oxide formed underlying the oxide layer.

104. (Previously presented) The semiconductor device of claim 88 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.

105. (Previously presented) The semiconductor device of claim 93 wherein the substrate comprises silicon.

106. (Previously presented) The semiconductor device of claim 105 further comprising an amorphous silicon oxide formed underlying the oxide layer.

107. (Previously presented) The semiconductor device of claim 93 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.

108. (Previously presented) The semiconductor device of claim 73 wherein the substrate comprises silicon.

109. (Previously presented) The semiconductor device of claim 108 further comprising an amorphous silicon oxide formed underlying the oxide layer.

110. (Previously presented) The semiconductor device of claim 73 wherein the oxide layer comprises an amorphous oxide formed by heat treating a monocrystalline oxide layer.--